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09/956,903	09/21/2001	Thomas D. Fletcher	2207/11270	2661

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EXAMINER	
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ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/956,903	FLETCHER, THOMAS D.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-21 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20,21,23 and 24* is/are allowed.

6)☒ Claim(s) *1-14 and 25-31* is/are rejected.

7)☒ Claim(s) *16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Appeal Brief filed 10/25/2006.

2. Claims 1-14, 16-21, and 23-31 are pending in this application. Claims 1, 4, 10, 20, and 25 are independent claims. During prosecution, claims 15 and 22 are cancelled. This Office Action is made non-final after considering the Appeal Brief filed 10/25/2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 4-13 and 25-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Winters (U.S. 6,466,960).

Re claim 4, Winters discloses in Figures 1 and 3 an apparatus (e.g. carry-save adder 10 in Figure 1) comprising a differential domino carry generate circuit (e.g. Figure 3A as carry circuit, col. 3 lines 4-11, and col. 4 line 64 to col. 5 line 10) having a first evaluation block of switches (e.g. as transistors 25 as switches in Figure 3A as the first evaluation block of switches) and a second evaluation block of switches (e.g. as transistors 26 as switches in Figure 3A as the second evaluation block of switches),

wherein the first evaluation block and second evaluation block each have the same number of switches connected in parallel (e.g. there are three parallel set of transistors in each blocks 25 and 26 in Figure 3A) and each have the same number of switches connected in series (e.g. there are two series set of transistors in each blocks 25 and 26 in Figure 3A), and wherein the circuit (e.g. circuitry in Figure 3A for producing carry signals) also has a true carry generate output (e.g. carry signal 29 in Figure 3A) and a compliment carry generate output (e.g. compliment carry signal 31 in Figure 3A) which both have an output drive strength (e.g. for driving the next circuit in line ZD 14 in Figure 1), and wherein the output drive strength for true output is the same as the output drive strength for compliment output (e.g. inherently as CARRYL is complemented version of CARRYH in Figure 3A and col. 5 lines 10-18).

Re claim 5, Winters further discloses in Figures 1 and 3 the switches in the first evaluation block and second evaluation block (e.g. transistors 25 and 26 in Figure 3A) are N-channel metal-oxide semiconductor (NMOS) transistors (e.g. col. 5 lines 1-10 and lines 34-41 for transistors 25 and 26).

Re claim 6, Winters further discloses in Figures 1 and 3 corresponding transistors in the first evaluation block and second evaluation block are the same size (e.g. there are five same transistors as NMOS for both block 25 and 26 in Figure 3A).

Re claim 7, Winters further discloses in Figures 1 and 3 the apparatus further comprises cross-coupled P-channel metal-oxide semiconductor (PMOS) keeper transistors (e.g. transistors 27-28 in Figure 3A).

Re claim 8, Winters further discloses in Figures 1 and 3 the differential domino carry generate circuit is a first stage in a carry look-ahead adder (e.g. stage 12 in Figure 1).

Re claim 9, Winters further discloses in Figures 1 and 3 the differential domino carry generate circuit is a group generate gate (e.g. Figures 1 and 3).

Re claim 10, Winters discloses in Figures 1 and 3 an apparatus (e.g. carry-save adder 10 in Figure 1 and corresponding circuitry in Figure 3A) comprising: a first output (e.g. output of transistor 35 in Figure 3A) to provide a precharge value during a precharge phase and a true carry generate value during an evaluation phase (e.g. output of transistor 35 in Figure 3A for charging the output signal CARRYH 31 prior entering inverter 24 in Figure 3A) ; a second output (e.g. output of transistor 34 in Figure 3A) to provide the precharge value during the precharge phase and the compliment of the true carry generate true during the evaluation phase (e.g. output of transistor 34 in Figure 3A for charging the output signal CARRYL 29 prior entering inverter 23 in Figure 3A); a current input (e.g. by transistor 33 in Figure 3A); a first evaluation block (e.g. all the transistors 25 in Figure 3A) connected to the current input (e.g. by transistors BH and AH in Figure 3A) and the second output (e.g. by transistors AH and CH in Figure 3A) and having a plurality of transistors (e.g. there are five transistors in the block 25 in Figure 3A), wherein a number of transistors are connected in a parallel relationship (e.g. transistors connect in parallel as {AH,BH}||{CH,AH}||BH as seen in Figure 3A) and a number of transistors are connected in a serial relationship (e.g. transistors connect in series as {AH-BH} and {CH-AH} in Figure 3A), wherein the first evaluation block (e.g. all transistors 25 in

Figure 3A) comprises a first transistor (e.g. transistor AH 25 in Figure 3A) with a drain connected to the second output, a second transistor (e.g. transistor BH 25 in Figure 3A) with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor (e.g. transistor CH 25 in Figure 3A) with a drain connected to the second output, a fourth transistor (e.g. transistor AH 25 in Figure 3A) with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with (e.g. transistor BH 25 in Figure 3A) a drain connected to the second output and a source connected to the drain of the fourth transistor (e.g. Figure 3A of cited reference is same as Figure 1 of present application); and a second evaluation block (e.g. all the transistors 26 in Figure 3A) connected to the current input (e.g. by transistor 33 in Figure 3A) and the first output (e.g. by transistor 35 in Figure 3A) and having a plurality of transistors (e.g. there are five NMOS transistors 26 in Figure 3A), wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block (e.g. transistors connect in parallel as {AL,BL}||{AL as should be CL,AL}||BL in Figure 3A) and the same number of transistors connected in a serial relationship as the first evaluation block (e.g. transistors 26 connect in series as {AL-BL} and {AL as should be CL-AL} in Figure 3A).

Re claim 11, Winters further discloses in Figures 1 and 3 the output drive strength for the first output is the same as the output drive strength for the second output (e.g. for driving the next circuit in line ZD 14 in Figure 1 and inherently as CARRYL is complemented version of CARRYH in Figure 3A and col. 5 lines 10-18).

Re claim 12, Winters further discloses in Figures 1 and 3 the circuit further comprises a clock input to receive a clock having precharge and evaluation phases (e.g. clock signal 32 in Figure 3A).

Re claim 13, Winters further discloses in Figures 1 and 3 the current input is a transistor (e.g. transistor 33 in Figure 3A) having a source node connected to ground (e.g. GND label of transistor 33 in Figure 3A) and a gate connected to the clock input (e.g. CLOCK label of transistor 33 in Figure 3A).

Re claim 25, Winters discloses in Figures 1 and 3 method (e.g. operation of circuitry in Figure 1 and 3B) comprising: receiving at a first evaluation block (e.g. all transistors 25 in Figure 3A) three true input values (e.g. AH, BH, and CH signal respectively as three true input values); receiving at a second evaluation block (e.g. al transistors 26 in Figure 3A) three compliment input values (e.g. AL, BL, and the last AL should be CL as noted with reference for correction in Figure 3A), wherein the compliment input values are the compliment of the true input values (e.g. col. 5 lines 10-18); processing the compliment input values at the second evaluation block to provide a carry generate value at a first output by selecting one of a plurality of stacks of transistors in the second evaluation block (e.g. output signal 31 as carry generate value by evaluated all the transistors 26 in Figure 3A), wherein each of stacks of transistors connects a current input to the first output (e.g. each stack of transistor {AL,BL}; {AL should be CL,AL}, and {BL} connects a current by the transistor 33 to the output signal 31 in Figure 3A); and processing the true input values (e.g. all true signals AH, BH, and CH are input respectively into the transistors 25 in Figure 3A) at the first evaluation block to

provide the compliment of the carry generate value at a second output (e.g. output signal 29 in Figure 3A) by selecting one of plurality of stacks of transistors in the first evaluation block (e.g. switching on/off the transistors 25 in Figure 3A), wherein each of stacks of transistors connects current input to the second output (e.g. each stack of transistor {AH,BH}; {CH,AH}, and {BH} connects a current by the transistor 33 to the output signal 29 in Figure 3A), and wherein the first evaluation block and second evaluation block have the same number of stacks of transistors (e.g. there are total three stack of transistors in each block 25 and 26 in Figure 3A).

Re claim 26, Winters further discloses in Figures 1 and 3 the first evaluation block and second evaluation block have corresponding stacks that have the same number of transistors (e.g. there are five transistors in each block 25 and 26; there area also three stack of transistors level in each bock 25-26 as seen in Figure 3A).

Re claim 27, Winters further discloses in Figures 1 and 3 the method further comprises: receiving a clock (e.g. CLOCK signal 32 in Figure 3A) having a precharge phase and an evaluation phase; providing precharge values at the first output and at the second output during precharge phase; and providing the compliment carry generate value at the first output and the carry generate value at the second output during the evaluation phase (e.g. output signals 29 and 31 respectively in Figure 3A).

Re claim 28, Winters further discloses in Figures 1 and 3 the method further comprises preventing current from passing through the current input during the precharge phase and enabling current to pass through the current input during the evaluation phase (e.g. Figure 3A).

Re claim 29, Winters further discloses in Figures 1 and 3 the method further comprises: providing the output from the first evaluation block to a keeper (e.g. output of transistors 25 into the transistor 27 in Figure 3A), providing the output from the second evaluation block to a keeper (e.g. output of transistors 26 into the transistor 28 in Figure 3A); and providing the carry generate true output (e.g. output signal 31 in Figure 3A) and carry generate compliment output (e.g. output signal 29 in Figure 3A) during the evaluation phase based upon output from the first evaluation block (e.g. block of transistors 25), second evaluation block (e.g. block of transistors 26), and the keeper (e.g. block of transistors 27-28).

Re claim 30, Winters further discloses in Figures 1 and 3 the inputs received and outputs provided are symmetrical (e.g. Figure 3A).

Re claim 31, Winters further discloses in Figures 1 and 3 the first evaluation block has three stacks of transistors (e.g. transistors 25 in Figure 3A wherein first stack {AH,BH}, the second stack {CH, AH}, and third stack {BH} in Figure 3A), and wherein the second evaluation block has three stacks of transistors (e.g. similarly transistors 26 in Figure 3A wherein first stack {AL,BL}, the second stack {AL as should be CL, AL}, and third stack {BL} in Figure 3A).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winters (U.S. 6,466,960) in view of Wickman et al. (U.S. 6,952,297).

Re claim 1, Winters discloses in Figures 1 and 3 an apparatus (e.g. carry-save adder 10 in Figure 1) comprising a symmetric differential domino carry generate circuit (e.g. Figure 3A as carry circuit, col. 3 lines 4-11, and col. 4 line 64 to col. 5 line 10) having true inputs and compliment inputs which both have a load (e.g. true inputs as AH, BH, CH and compliment inputs as AL, BL, CL as seen in Figure 3A and col. 5 lines 10-18 wherein the suffixed H and L represent or symbolize the true and complemented input signal respectively); noted the "AL" label for transistor 26 should be "CL" for correction as seen in Pfennings (U.S. 4,667,303)). Winters does not explicitly define or illustrate the load for the true inputs is equal to the load for the compliment inputs. However, Wickman et al. explicitly disclose that the load for the true inputs is equal to the load for the compliment inputs (e.g. col. 3 lines 7-14 and col. 4 lines 42-45). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to have the load for the true inputs is equal to the load for the compliment inputs as clearly taught in Wickman et al.'s invention into Winters' invention because it would enable to improve the speed of producing the resultant (e.g. col. 1 lines 25-33 and col. 1 lines 36-51).

Re claim 2, Winters further discloses in Figures 1 and 3 the circuit also has a true carry generate output (e.g. signal at point 29 in Figure 3A) and a compliment carry generate output (e.g. signal at point 31 in Figure 3A) which both have an output drive

strength (e.g. for driving the next circuit in line ZD 14 in Figure 1), and wherein the output drive strength for true output is the same as the output drive strength for compliment output (e.g. inherently as CARRYL is complemented version of CARRYH in Figure 3A and col. 5 lines 10-18).

Re claim 3, Winters further discloses in Figures 1 and 3 the circuit further a first evaluation block having a plurality of transistors (e.g. all transistors 25 in Figure 3A), wherein a number p of transistors are connected in a parallel relationship (e.g. p is equated to 3 as transistors AH & BH are in parallel with transistors CH & AH and transistor BH in Figure 3A) and a number s of transistors are connected in a serial relationship (e.g. s is equated to 2 as transistor AH is series with transistor BH in Figure 3A); and a second evaluation block having a plurality of transistors (e.g. all transistors 26 in Figure 3A), wherein in the second evaluation block p transistors are connected in a parallel relationship and s transistors are connected in a serial relationship (e.g. similar structure as seen on the left side as first evaluation block in Figure 3A).

Re claim 14, Winters further discloses in Figures 1 and 3 the gate of each transistor in the first evaluation block is connected to one of a set of true inputs (e.g. all transistors 25 have gates connected to all true signals as AH, BH, and CH as seen in Figure 3A) and the gate of each of the transistors in the second evaluation block is connected to one of a set of compliment inputs (e.g. all transistors 26 have gates connected to all complemented signals as AL, BL, and CL as seen in Figure 3A, as noted above the label for AL below transistor 28 should be CL for correctness). Winters does not explicitly define or illustrate the load for the true inputs is equal to the load for the

compliment inputs. However, Wickman et al. explicitly disclose that the load for the true inputs is equal to the load for the compliment inputs (e.g. col. 3 lines 7-14 and col. 4 lines 42-45). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to have the load for the true inputs is equal to the load for the compliment inputs as clearly taught in Wickman et al.'s invention into Winters' invention because it would enable to improve the speed of producing the resultant (e.g. col. 1 lines 25-33 and col. 1 lines 36-51).

Allowable Subject Matter

7. Claims 20-24 are allowed.

8. Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to claims 1-14 and 25-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,667,303 to Pfennings discloses a digital integrated circuit comprising complementary field effect transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

May 8, 2007

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